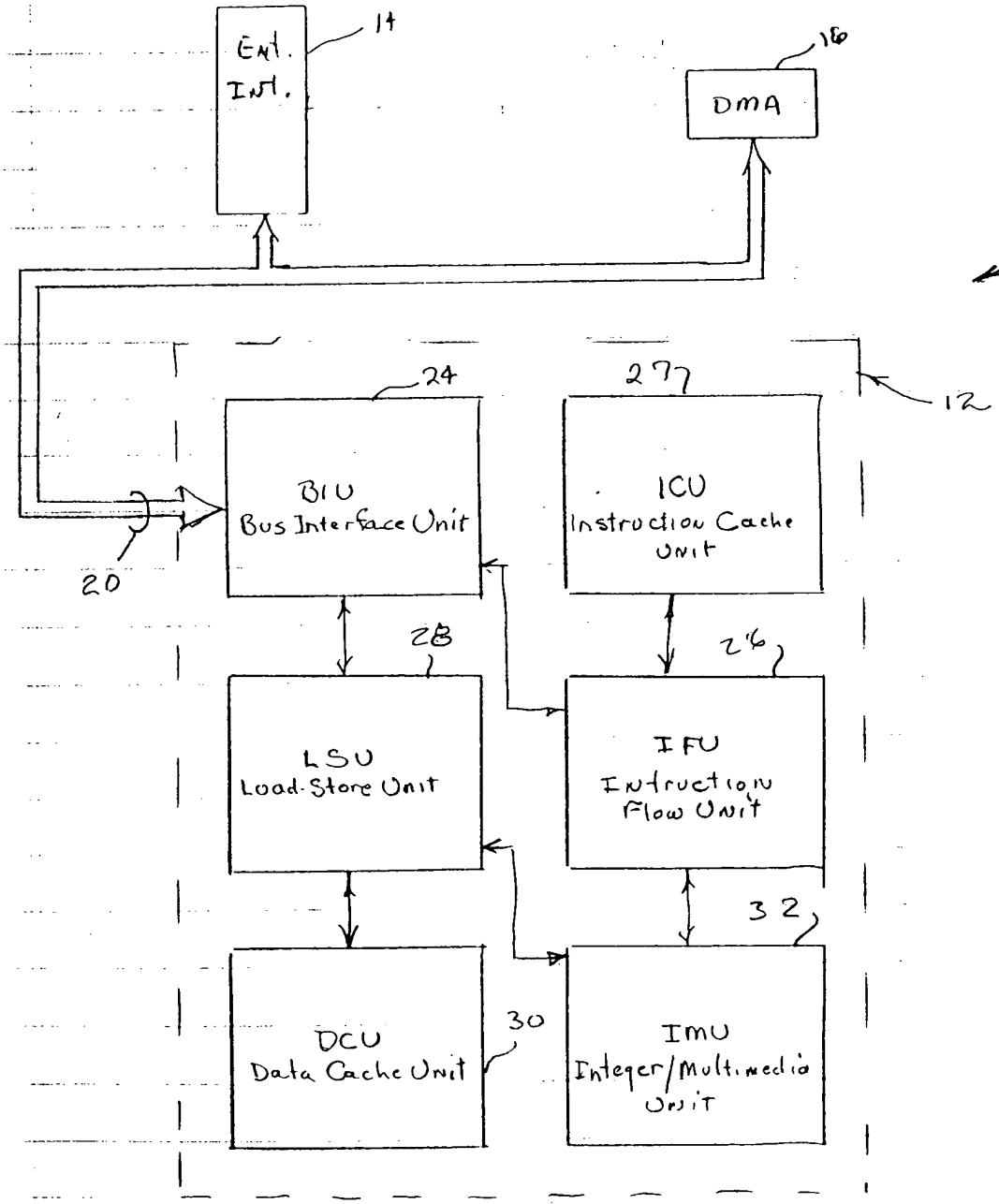
Ext. Int.
14
DMA
16
10
12
24
27
BIU
Bus Interface Unit
ICU
Instruction Cache Unit
20
28
26
LSU
Load-Store Unit
IFU
Instruction Flow Unit
32
DCU
Data Cache Unit
30
IMU
Integer/Multimedia Unit

FIG-1

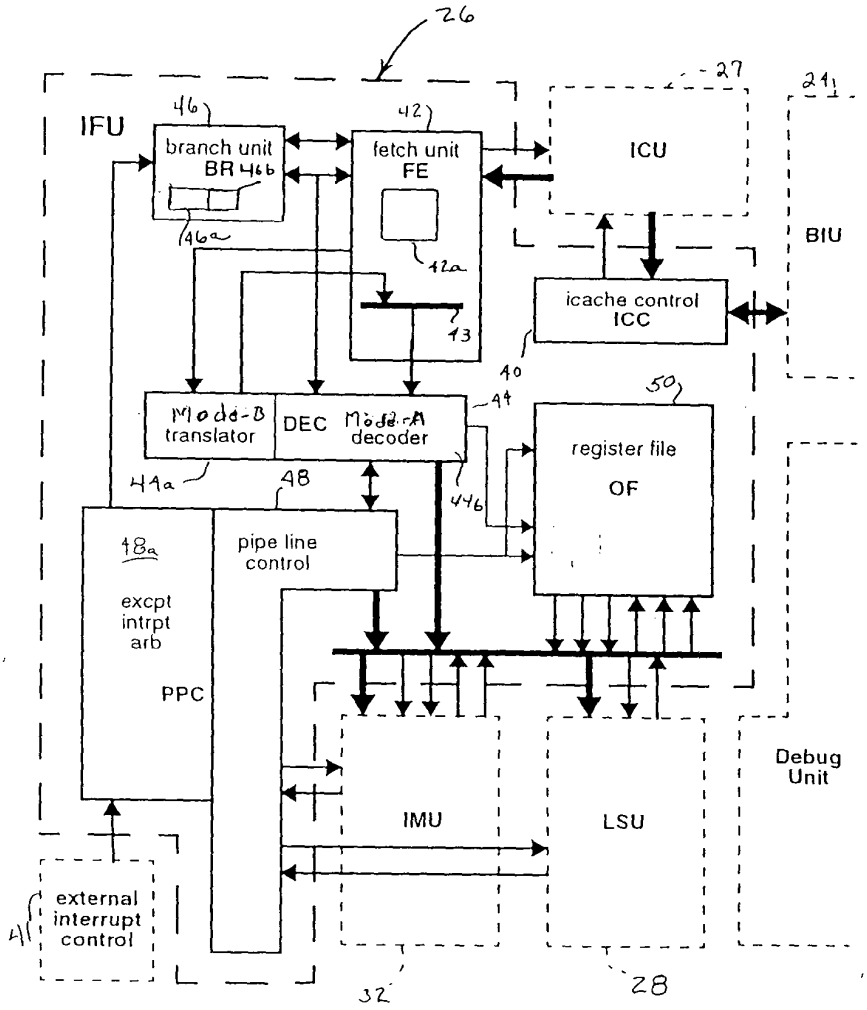
26
IFU
46
branch unit
BR 46b
46a
42
fetch unit
FE
42a
13
27
ICU
21
BIU
icache control
ICC
40
Mode-B
translator
DEC
Mode-A
decoder
44
50
register file
OF
44a
48
44b
18a
pipe line
control
excpt
intrpt
arb
PPC
IMU
LSU
Debug
Unit
external
interrupt
control
41
32
28

FIG_2

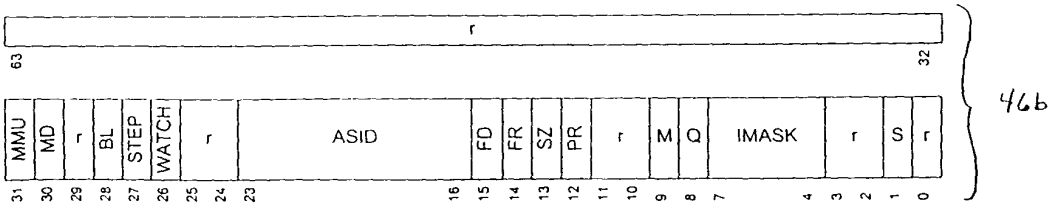
r
63
32
MMU
MD
r
BL
STEP
WATCH
r
ASID
FD
FR
SZ
PR
r
M
Q
IMASK
r
S
r
31
30
29
28
27
26
25
24
23
16
15
14
13
12
11
10
9
8
7
4
3
2
1
0
46b

FIG_3

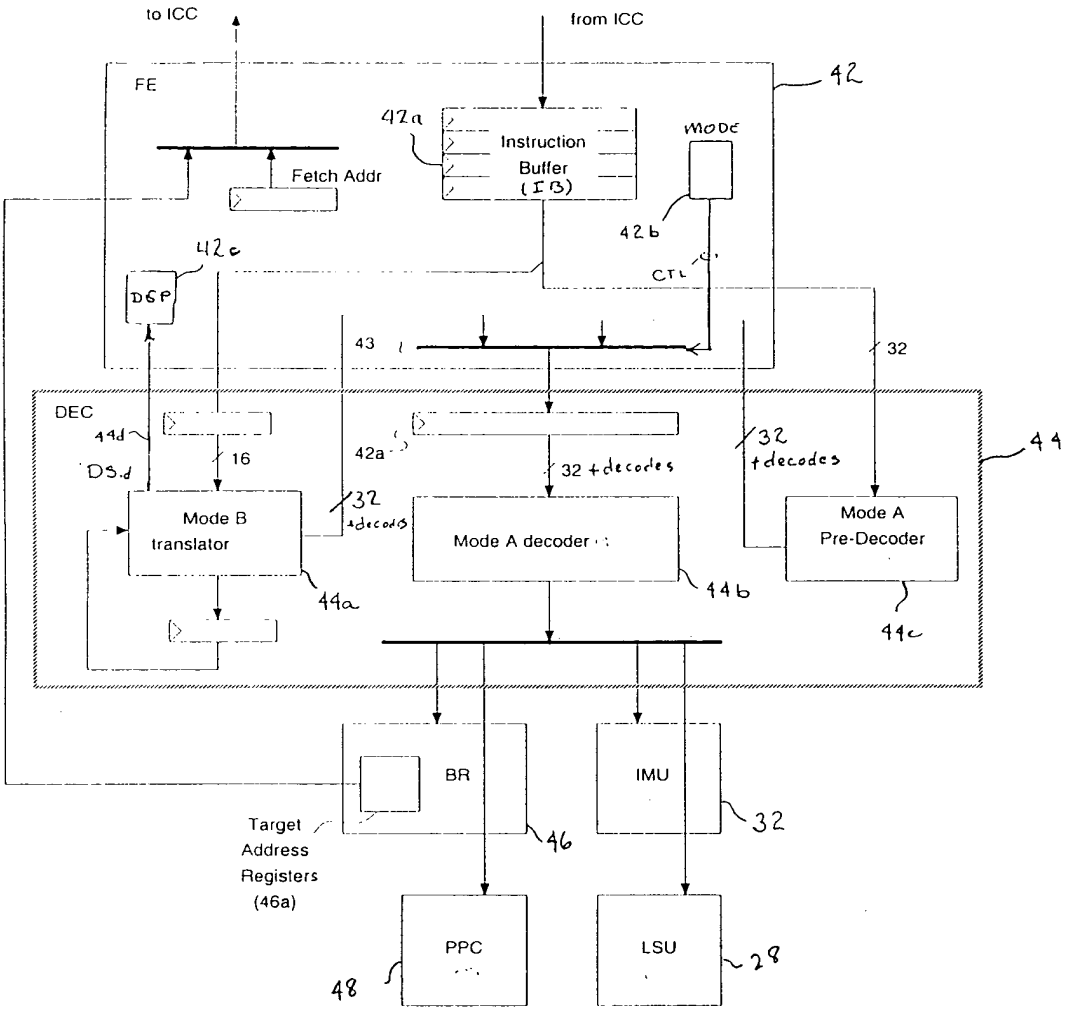


FIG_4

| MODE B STATE | DESCRIPTION | MODE A STATE |
|---|---|---|
| PC | Program counter | Lower 32 bits of PC |
| Ri where i is in [0, 15] | Mode B general-purpose registers | Lower 32 bits of $R_i$ where i is in [0, 15] |
| PR | Procedure link register | Lower 32 bits of $R_{18}$ |
| GBR | Global base register | Lower 32 bits of $R_{27}$ |
| MACL | Multiply-accumulate low | Lower 32 bits of $R_{24}$ |
| MACH | Multiply-accumulate high | Upper 32 bits of $R_{24}$ |
| T | Condition code flag | Bit 0 of $R_{25}$ |
| S | Multiply-accumulate saturation flag | SR.S |
| M | Divide-step M flag | SR.M |
| Q | Divide-step Q flag | SR.Q |

FIG_5

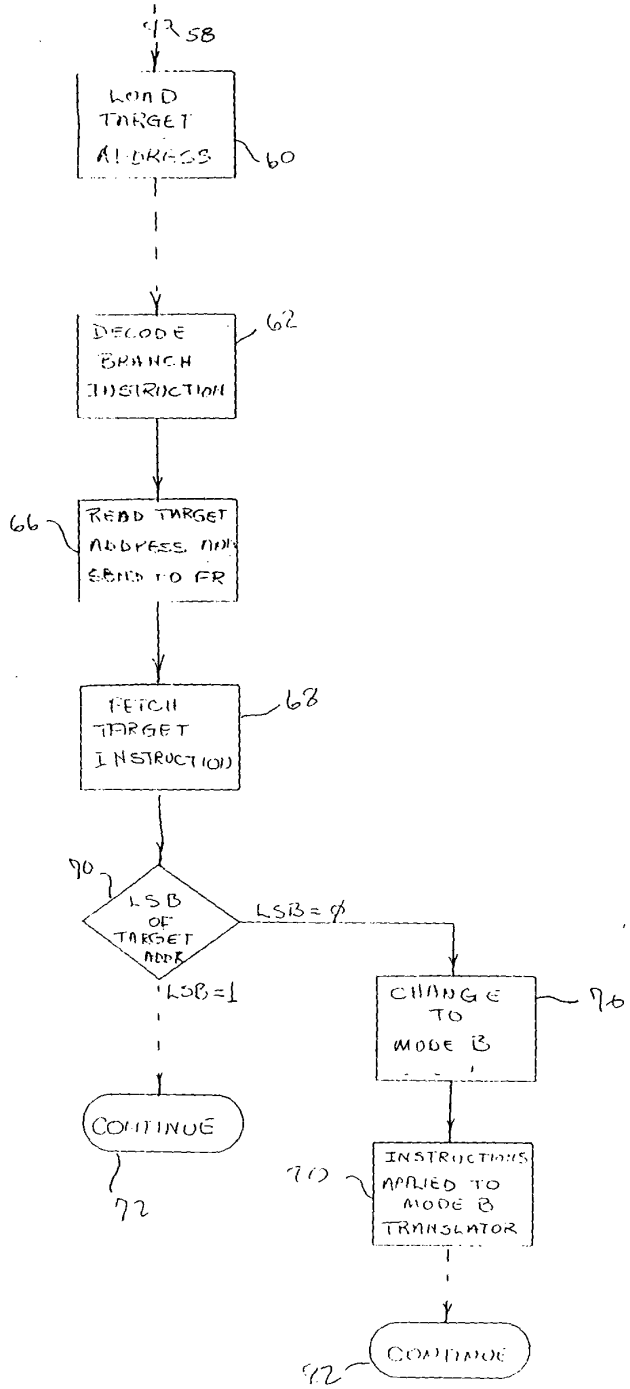
58
LOAD TARGET ADDRESS
60
DECODE BRANCH INSTRUCTION
62
66
READ TARGET ADDRESS
68
FETCH TARGET INSTRUCTION
70
LSB OF TARGET ADDR
LSB = 0
LSB = 1
CHANGE TO MODE B
76
CONTINUE
72
INSTRUCTIONS APPLIED TO MODE B TRANSLATOR
74
CONTINUE
72

FIG-6